System Memory
Resident Blocks

MR WF E Table

Data Buffer

Send Queue

Receive Queue

PCounrol lock

Complete Queue

Event Queue

C Pa e Table

Pa e Table

System Memory

Processor CPU

System Interconnect

STORAGE MEDIUM

34

30

32

Initialized by Platform Dependent Means

MRWPT Table

General Base Address Register

General Registers

Part 1 Context

PartN Context

QP Contexts

CQ Contexts

EQ Contexts

18

16

16

16

12

22

18

20

14

10

FIGURE 1

The following figures illustrate conceptual details of parts of the overall resource-address-translation flow.

Adapter-Type / Adapter-ID to Adapter-Resource Table Address

FIG. 2A

RT	ART_Example
00	ART Entry$_0$
01	ART Entry$_1$
02	ART_Example Entry for CQ Resource Type
03	
	. . .
FF	ART Entry$_{255}$

Adapter Resource Table (ART)

FIG. 2B

ART_Example Entry for CQ Resource Type

DWord						
0	ASAB		PRC		MRC	
1	SAC	Reserved	SMC		Reserved	
2	Reserved	LARID		Reserved	RIL	
3	Access-Table Address (ATA) - AT is for all CQ Resources					Reserved
4	Adapter-Storage Base Address for SAT=0					Reserved
5	Adapter-Storage Base Address for SAT=1					Reserved
6-18	. . .					Reserved
19	Adapter-Storage Base Address for SAT=15					Reserved

Bits: 0   8   16   32   40   62   63

Figure 2C Adapter-Resource-Table Entry (ARTE).

Figure 3 Resource Address Translation.

CQ Access Table (AT=0, AID=0)

	PSC	SIEC	M	P	V	PT	RZONE	GOID	PID
CQ0	0	0000	0	1	1	0	00	000	0000
CQ1	0	0000	0	1	1	0	00	000	0000
CQ2	1	3000	0	0	1	1	03	012	FF00

CQ Adapter-Resource-Table Entry
AT=0, AID=0

	SAC	PRC	ATA	SPSAA	RSAA	PSAA	USAA
CQ	5	2	AF000	1A000	2A000	3A000	4A000

RID=2 ⊗ 4K

(02000)

STORE MEMORY MAPPED I/O
Resource-Address Designation:
AID = 0 (HCA 0)
RT = 2 (CQ), RID = 2 (CQ2)
SAT = 2 (Privileged-Storage Area)
SAO = 008 hex

⊕

(3C000)

SAO=008 hex → ⊕   HSA

- -

HCA Address Space

CQ Privileged-Storage-Area
Address

CQ0-3A000

CQ1-3B000

CQ2-3C000

3C008